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Analysis of Low Phase Noise and Low Power CMOS VCO – A Review

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***Abstract*- Four different topologies of VCO near 100 GHz for low power consumption and low phase noise are studied in this paper. After comparing these different topologies of VCO, it is seen that complementary LC VCO provides minimum power consumption of 7.59 mW at 32 nm CMOS technology and VCO with optimum pumping method provides minimum phase noise of -85 dBc/Hz @10MHz.**

***Keywords*-Phase noise, power consumption, VCO, CMOS.**

I. INTRODUCTION

These days the transfer of large amount of data is required at high speed. These parameters of telecommunication can only be achieved using very fast clock of the processor. These circuits must be designed using MOSFET technology so as to be operated at high frequencies and high power [21][3]. Also, these high-speed communication systems are advancing by using CMOS processes. For the generation of clock in communication systems, a phase locked loop with a voltage controlled oscillator is used [16].

II. NEED FOR 100 GHZ OPERATING FREQUENCY

As the data traffic in communication is increasing day by day, the requirement for high data transfer in communication systems has been emerged. Due to this, the requirement of increased bandwidth is needed for communication systems. By using high carrier frequency, wider bandwidth can be produced and thus systems which operate at frequencies beyond 100 GHz are becoming popular these days [19].

III. VCO BASIC

A voltage controlled oscillator (VCO) is the most important part in analog and digital communication systems. The need for the high operating frequency can be achieved by using VCOs. VCOs using CMOS technology are being used to allow oscillators to achieve gigahertz range frequencies [18][1].The traditionally used two types of VCOs are Complementary metal oxide semiconductor (CMOS) ring oscillator and Inductor-capacitor (LC) tank based oscillator [17][4][5].

A. LC VCO Basic

A general LC-VCO shown in Fig.1 consists of a parallel resonance tank with inductance L and capacitance C. RL and RC are the parasitic resistances of L and C, respectively. To compensate the losses due to RL and RC, active components such as CMOS transistors are used to realize a negative resistance $-R$. The loss in the tank is given by:

$$Ploss = 4\pi^2 RC^2 f0^2 Vpeak^2 = \frac{R}{4\pi^2 L^2 f0^2} Vpeak^2 \quad \text{--- (1)}$$

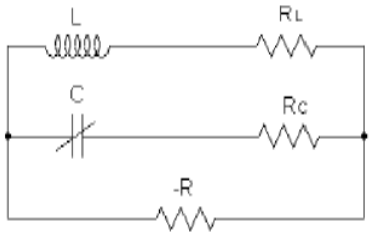

Fig. 1 LC VCO

Where R represents the combined losses of the inductance and the capacitance, and Vpeak is the peak voltage amplitude across the capacitance. It can be observed from (1) that the power loss decreases linearly with the series resistance in the resonance tank, and it also decreases quadratically with an increase of the tank inductance [6]. For the resonance tank to resonate without any loss, the parasitic resistance coming from both the inductor and capacitor must be compensated. To compensate the parasitic resistance, a negative resistance -R is formed in the tank circuit so that both of the parasitic resistances can be cancelled out. But in actual, the negative resistance does not exist. A negative resistance is formed by connecting cross-coupling transistors to the resonant tank. Figure 2 shows such a circuit.

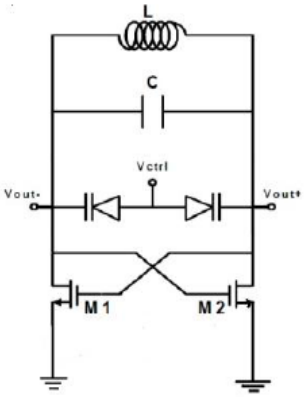

Fig. 2 Cross coupled oscillator

By cross-connecting the output to the input of the oscillator, negative resistance is created which has the same conductance as the transistor's transconductance (gm) [15].

B. Ring VCO Basic

A ring oscillator is formed by using a number of delay stages, in which the output of the last stage is fed back to the input of the first stage. For oscillation, the circuit must provide a phase shift of 2π and must have unity voltage gain at the oscillation frequency [18].

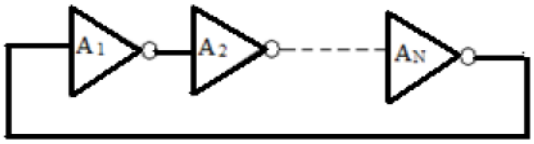

Fig. 3 Ring oscillator

Every delay stage introduces a phase shift of π=N, where N is the number of delay stage. Whereas the remaining phase shift is introduced by a dc inversion. Thus for an oscillator with single-ended delay stages, an odd number of stages is the condition for the dc inversion [2].

C. Comparison Between Lc Vco And Ring Vco

The Voltage controlled oscillators have a very important role in PLL (Phase Lock Loop) circuit. Two commonly used VCOs are CMOS ring oscillator and LC tank oscillators. The LC oscillator circuits have better noise characteristics, but these have large dimensions and are not suitable for the phase shift operation. Whereas the ring VCO has the very good performance over LC oscillator because of its low power requirements and less area on the chip but it is more prone to noise. Due to this reason, ring oscillators are more widely used [22] [20].

IV. PARAMETERS OF VCO

There are a number of specifications available for VCO performance such as oscillation frequency, frequency tuning range, phase noise at a particular offset frequency and power consumption. However a problem exists between power consumption and phase noise.

A. FOM (figure-of-merit)

For the comparison purpose of the performance of two VCOs figure of merit is calculated. The general Figure-Of-Merit (FOM) formulas is expressed as

$$FOM = L(\Delta w) - 20.\log\left[\left(\frac{w_0}{\Delta w}\right)\right] + 10.\log\left(\frac{P_{diss}}{1mW}\right) \quad (2)$$

Which includes phase noise $L(\Delta\omega)$ at an offset frequency of Δω, oscillation frequency $\omega 0$ and power consumption of the circuit P_{diss} [11].

B. Phase noise

The noise is added into an oscillator by the devices that constitute active and passive elements [9]. This noise alters both the amplitude and frequency of oscillation. Amplitude noise is not so important because the non-linearities that affect the amplitude of oscillation also stabilize the amplitude noise. But the phase noise is a random deviation in frequency which can be viewed as a random variation in the zero crossing points of the time-dependent waveform of the oscillator. For an ideal oscillator, the output can be expressed as:

$$Vout = A\cos\left[\omega_o t + \varphi\right] \quad \text{---------(3)}$$

Where amplitude A and arbitrary phase φ are constant values. However for a real oscillator, the amplitude and the phase are affected by noise and are time-variant due to which the output becomes:

$$V_{out}(t) = A(t)\cos[w_o t + \emptyset(t)] \quad \text{------------(4)}$$

Where φ(t) is the excess phase of the output [10].

C. Voltage Controlled Frequency Tuning

In today's era, the wireless systems require a tunable oscillator, in which the output frequency is a function of a control input. In an ideal VCO, the output frequency is a linear function of its control voltage (*Vcon*) [9],

$$f_{out} = f_0 + K_{VCO}.V_{con} \quad \text{-------(5)}$$

Where, *f*o is the oscillation frequency at *Vcon* = 0 and K_{VCO} is the gain or sensitivity of the circuit. The range, *f2 – f1*, is called the frequency tuning range.

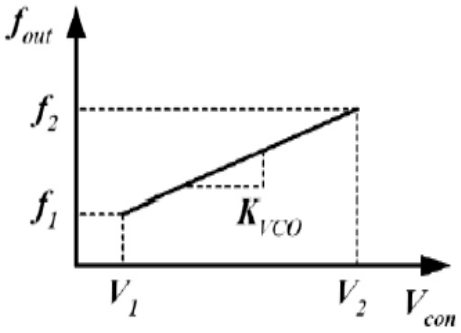

Fig. 4 Definition of KVCO

The frequency tuning is required to occupy the whole application bandwidth. The oscillation frequency of an LC-tank VCO is equal to

$$f_{osc} = 1/(2\pi\sqrt{LC}) \quad \text{----------(6)}$$

That means only the values of inductor and capacitor can be varied to tune the oscillation frequency.

D. Power Consumption

For the applications of communication systems, low power consumption is needed. As the phase noise is inversely proportional to the power dissipated in the resistive part of the resonant LC tank circuit. This means that a small phase noise can be achieved by increasing the bias current within the practical limitations. With the increase in bias current, the VCO's output voltage amplitude will be increased. But the CMOS transistor has a maximum voltage range that cannot be exceeded to avoid permanent damage [12].

V. VCO TOPOLOGIES NEAR 100 GHZ

The Voltage Control Oscillator (VCO) is a building block for communication systems. Low phase noise, low power consumption and best FOM are the main objectives of an ideal VCO.

A. NMOS cross coupled LC tank VCO

In this, a 94 GHz VCO using low leakage transistors in 65 nm digital CMOS processed with 6 metal layers. In figure,

VCO is a simple NMOS cross-coupled pair. The NMOS transistor's width and length are sized to obtain sufficient negative resistance and maximum frequency at targeted bias current. As the tail current source, a PMOS transistor is used. Its larger gate area reduces the 1/f noise and phase noise of VCO. The PMOS transistor current can be controlled with the loop-filtered control voltage in a PLL to change the dc drain voltage of the cross-coupled pair so that the VCO tuning range can be enhanced. The output power varied between -4 and -8 dBm over the tuning range. The VCO could be tuned from 91.8 to 97.4 GHz which should be sufficient to tolerate the capacitance and positive variations resulting from the process variations [13].

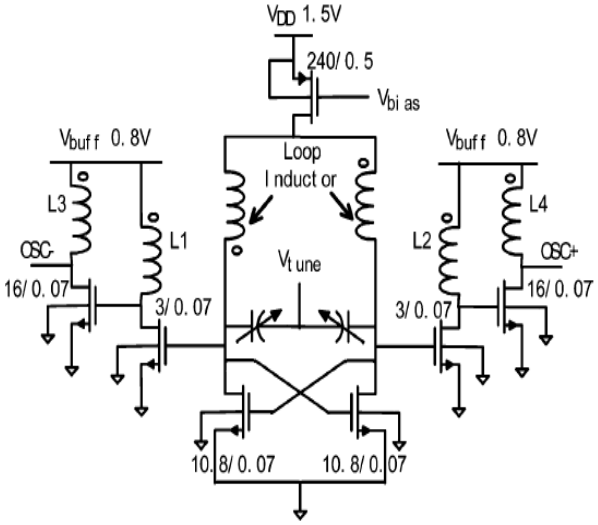

Fig. 5 NMOS cross coupled LC tank VCO

B. *VCO with fourth order LC resonator*

In this, the high speed voltage controlled oscillator (VCO) in 65 nm CMOS technology has been achieved. The VCO with fourth order LC resonator has implemented. The VCO oscillates at the secondary resonant pole of its LC resonator. It has achieved a frequency enhancement of 84.7% while compared with a conventional cross-coupled VCO. This VCO has been incorporated in phase locked loop (PLL) to generate the clock signals above 100 GHz. The measured tuning range for this VCO is from 103.057 to 104.581 GHz [16].

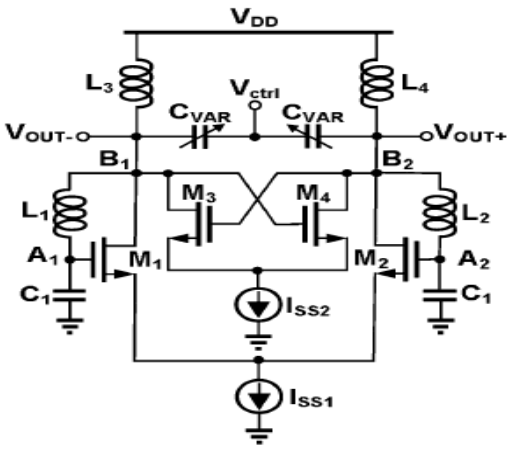

Fig. 6 VCO with fourth order LC resonator

C. *VCO using optimum pumping method*

In this, 90nm high performance CMOS technology has been used that provides transistors which are stable at frequencies in millimeter-wave range. This stability allowed the usage of simultaneous complex conjugate matching at input and output ports of every transistor in the VCO. Due to this matching, energy pumps from the active device to the passive network (optimal pumping). Depending on the transistor technology, the number of stages that are required for a multiple of 360° phase shift in the signal is high. The transistor S-parameters were used to 64GHz and 100GHz [7].

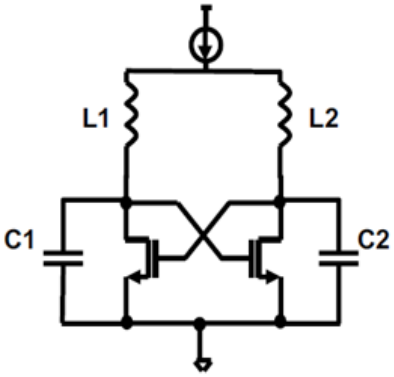

Fig. 7 VCO using optimum pumping method

D. *Complementary LC VCO*

The presented complementary LC-VCO is attractive for VCO arrays. It has used an LC-tank and its area is minimal and highly scalable. The nanometer CMOS technology is used to retain high-speed design margin for mm-wave circuit. For higher oscillation frequency, multiple-harmonic VCOs have been implemented, but they don't have active components that can operate very fast to implement a practical transceiver system. The complementary LC-VCO design, shown in Figure, is the cross-coupled inverter topology which allows more balanced and symmetric VCO output swing so as to improve phase noise performance and power consumption. It has also showed symmetric varactor and VCO tuning with the varactor biasing. SOI CMOS technology has been implemented for high-frequency VCOs with a wide-tuning capability. The implemented VCOs are able to tune from 83.20 to 96.98GHz [14].

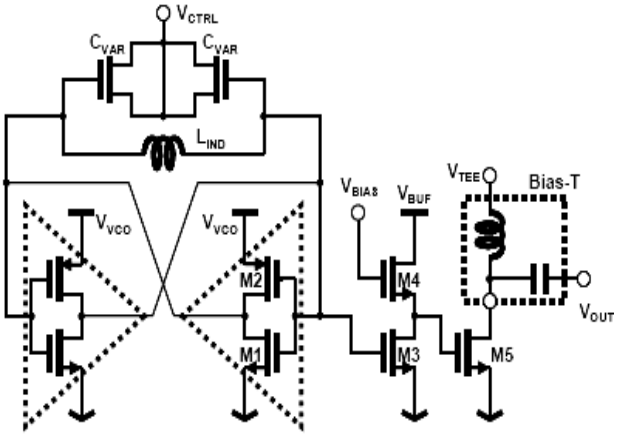

Fig. 8 Complementary LC VCO

VI. COMPARISON AND DISCUSSION

From this comparison table, it is seen that when we compared, 64 GHz, 94 GHz, an array and base paper, the phase noise of first is minimum as compare to others. Also the power consumed by an array is minimum i.e 7.59 mW.

TABLE 1 COMPARISON OF PARAMETERS

Mode	Ref. 7	Ref. 13	Ref. 14	Ref. 16
Technology	90nm CMOS	65nm CMOS	32nm CMOS	65nm CMOS
Tuning Range(GHz)	103.9 -105.9	94 -97.4	100.07 -104.28	103.06 -104.58
Supply voltage	1V	1.5V	1.2V	1.2V
FOM	-150.2 dBc/Hz	-175.9 dBc/Hz	-172.45 dBc/Hz	-170.62 dBc/Hz
Power consume	30mW	9mW	7.59mW	12mW
Phase noise(@10MHz)	-85 dBc/Hz	-106 dBc/Hz	-100.88 dBc/Hz	-101.08 dBc/Hz
Carrier frequency	--	94.92 GHz	102.2 GHz	100 GHz
Current consume	30mA	6mA	--	--

VII. CONCLUSION

For four different topologies of VCO, phase noise and power consumptions have been compared. From this it is studied that as the supply voltage increases, FOM also increases. Also with the increase in phase noise, the power consumption decreases.

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